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Control Strategy for Three Phase PWM Rectifier Using SVM Modulation

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***Abstract*— This paper deals with the control of three phase PWM rectifier model using SVM based current controller. In many power electronics control applications the rectifier plays vital role during AC/DC power conversion. The SVM-based HCC scheme is simulated using MATLAB simulink. The technique combines the best features of the SVM and HCC techniques. The controller determines a set of state space vectors from a region detector and then applies a space vector selected according to HCC. A set of space vectors in a region, including the zero space vector for a reduced number of switching, is determined from the output signals of three comparators with a hysteresis band a little larger than that of the main HCC. The Simulation results prove the effectiveness of the proposed three phase PWM rectifier model.**

Keywords- PWM Rectifier. SVM, HCC

I. INTRODUCTION

The increase in use of electronic equipments such as computers, radio set, printers, TV sets, etc., acts as nonlinear loads, are source of current harmonics, which leads to increase in reactive power and power losses in transmission lines. The harmonics also cause electromagnetic interference and, sometimes, dangerous resonances. They have negative influence on the control and automatic equipment, protection systems, and other electrical loads, resulting in reduced reliability and availability. Moreover, non-sinusoidal currents produce non sinusoidal voltage drops across the network impedances, so that a non-sinusoidal voltage appears at several points of the mains. It brings out overheating of line, transformers and generators due to the iron losses.Reduction of harmonic content in line current to a few percent allows avoiding most of the mentioned problems. Restrictions on current and voltage harmonics maintained in many countries through IEEE 519-1992 and IEC 61000-3-2/IEC 61000-3-4 standards, are associated with the popular idea of clean power. Methods for limitation and elimination of disturbances and harmonic pollution in the power system have been widely investigated by many researchers. These techniques based on passive components, mixing single and three-phase diode rectifiers, and power electronics techniques as: multi pulse rectifiers, active filters and PWM rectifiers.

They can be generally divided as:

- Harmonic reduction of already installed non-linear load;
- Harmonic reduction through linear power electronics load installation.

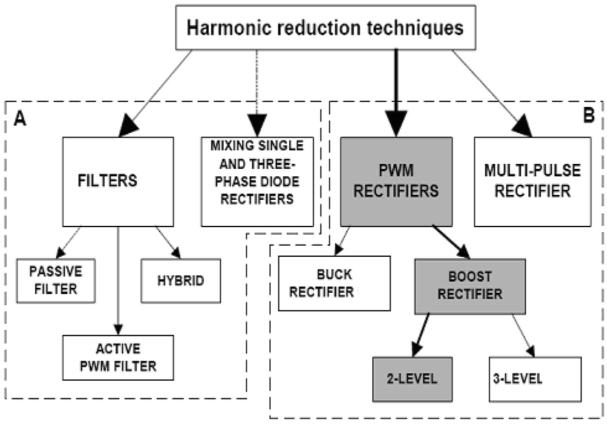


Figure 1. Most popular three-phase harmonic reduction techniques of Current

- Harmonic reduction of already installed non-linear load
- Harmonic reduction through linear power electronics load installation.

Traditional method of current harmonic reduction involves passive filters LC, parallel-connected to the grid. Filters are usually constructed as series-connected legs of capacitors and chokes. The number of legs depends on number of filtered harmonics (5th, 7th, 11th, and 13th). The advantages of passive filters are simplicity and low cost. The disadvantages are:

- Each installation is designed for a particular application (size and placement of the filters elements, risk of resonance problems),
- High fundamental current resulting in extra power losses,

- Filters are heavy and bulky.

The other technique, based on mixing single and three-phase non-linear loads, gives a reduced THD because the 5th and 7th harmonic current of a single-phase diode rectifier often are in counter-phase with the 5th and 7th harmonic current of a three-phase diode rectifier. The power electronics techniques are use of multipulse rectifiers. Although easy to implement, possess several disadvantages such as: bulky and heavy transformer, increased voltage drop, and increased harmonic currents at non-symmetrical load or line voltages.

An alternative to the passive filter is use of the shunt active PWM filter, which displays better dynamics and controls the harmonic and fundamental currents. Active filters (AF) are mainly divided into two different types: the active shunt filter (current filtering) and a PWM (active) rectifier is shown in Fig.1.

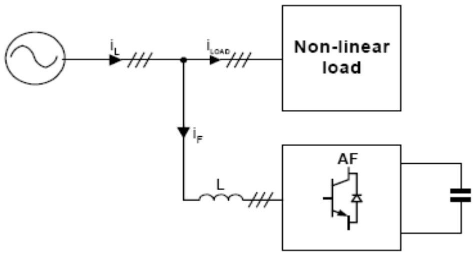


Figure 2. Three-phase shunt Active filter

The three-phase two-level shunt AF consists of six active switches and its topology is identical to three phase PWM converter. The Active Filterrepresents a controlled current source $i_F$which added to the load current i_{Load}yields sinusoidal line current i_L(Fig. 2). Active filter provides:

- Compensation of fundamental reactive components of load current,
- Load symmetrization (from grid point of view),
- Harmonic compensation much better than in passive filters.

In spite of the excellent performance active filters possess certain disadvantages such as complex control, switching losses and EMC problems. For reduction of these effects, a small low-pass passive filter between the line and the AF is necessary.

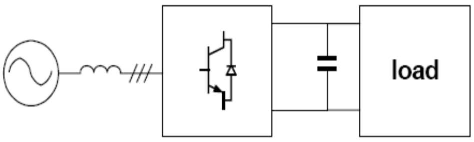
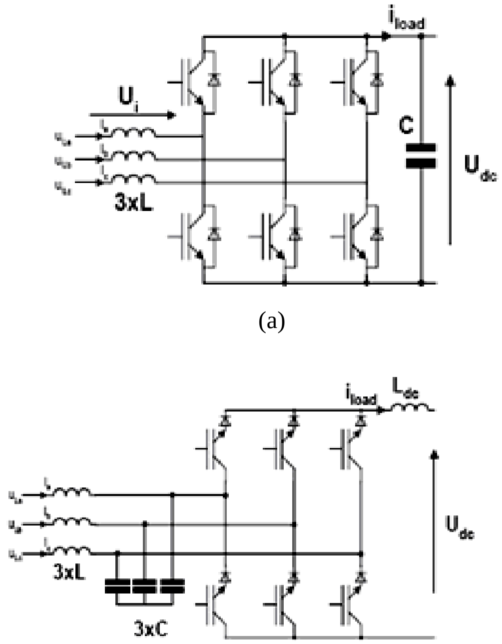


Figure 3. PWM rectifier

The other current harmonic reduction technique is a PWM (active) rectifier (Fig.3). PWM rectifiers can be configured as a voltage source output (Fig.4a) and a current source output (Fig. 4b). Voltage source configuration is aboost rectifier (increases the voltage) works with fixed DC voltage polarity, and the current source configuration is a buck rectifier (reduces the voltage) operates with fixed DC current flow.



(a)

Figure 4. (a) Boost topology of PWM rectifier (b) Buck topology of PWM rectifier

Important features of PWM rectifiers are:

- Bi-directional power flow,
- Nearly sinusoidal input current,
- Regulation of input power factor to unity,
- Low harmonic distortion of line current (THD below 5%),
- Adjustment and stabilization of DC-link voltage (or current)

II. OVERVIEW OF THE PAPER

The basic block diagram of the proposed technique is shown in the fig.1.It consists of input circuit, region detector, PWM rectifier circuit,SVM-based HCC algorithm and the voltage controller. The input circuit is three phase ac supply. The integration amplifier amplifies the input supply and is given to the region detector and the normaliser. The integration amplifier amplifies the input supply and is given to the region detector and the normaliser. The region detector is utilised to detect the region where the reference voltage lies.

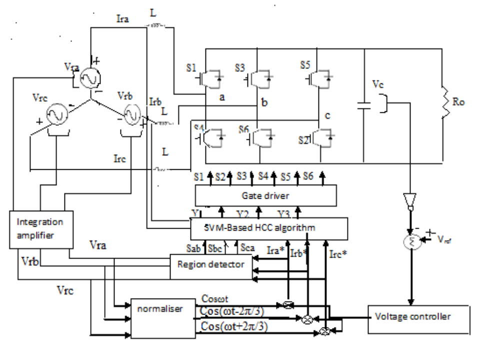


Figure 5. Block diagram of the proposed SVM-Based HCC controller

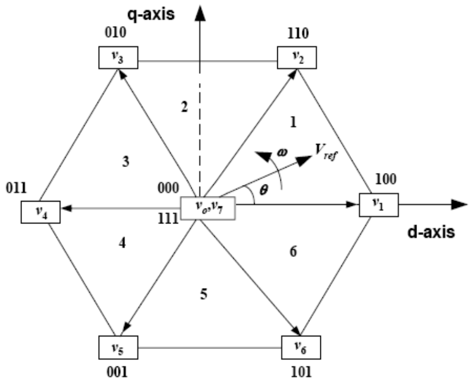


Figure 6. Space vectors generated by the SVPWM

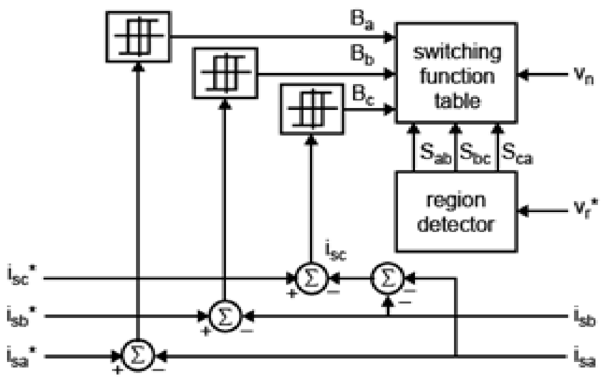


Figure 7. Block diagram of the proposed controller.

As shown in Fig. 7, three hysteresis comparators are used to track the current command vector and limit the current error within the specified bound. B denotes a status of the bound of the a-axis current error. The space vectors V0, V1 and V2 in region 1 are utilized as in the SVM technique, as shown in Fig.3b. When the current error of the a-axis hits the upper bound of the hysteresis comparator and the current error of the b-axis hits the lower bound, Ba = 1 and Bb =0. The voltage vector V1 is applied to increase the b-axis current ib and c-axis current ic simultaneously when Bb = 1 and Bc =1.

III. PWM RECTIFIER AND MODULATION TECHNIQUES

A voltage source PWM inverter with diode front-end rectifier is one of the most common power configuration used in modern variable speed AC drives (Fig. 8). An uncontrolled diode rectifier has the advantage of being simple, robust and low cost. However, it allows only unidirectional power flow. Therefore, energy returned from the motor must be dissipated on power resistor controlled by chopper connected across the DC link. The diode input circuit also results in lower power factor and high level of harmonic input currents. A further restriction is that the maximum motor output voltage is always less than the supply voltage. Equations (2.1) and (2.2) can be used to determine the order and magnitude of the harmonic currents drawn by a six-pulse diode rectifier:

$$h=6k\pm1 \qquad k=1,2,3 \tag{2.1}$$

$$\frac{I_h}{I_1}=\frac{1}{h} \tag{2.2}$$

Harmonic orders as multiples of the fundamental frequency, 5th, 7th, 11th, 13th etc., with a 50 Hz fundamental, corresponds to 250, 350, 550 and 650 Hz, respectively. The magnitude of the harmonics in per unit of the fundamental is thereciprocal of the harmonic order: 20% for the 5th, 14% for the 7th, etc. Equations (2.1) and (2.2) are obtained from the Fourier series for an ideal square wave current (critical assumption for infinite inductance on the input of the converter). Equation (2.1) is fairly good description of the harmonic orders generally encountered. The magnitude of actual harmonic currents often differs from the relationship described in (2.2). The shape of the AC current depends on the input inductance of converter. The ripple current is equal 1/L times the integral of the DC ripple voltage. With infinite inductance the ripple current is zero and the input current is flat-top wave.

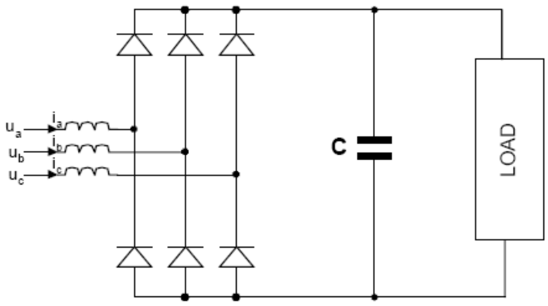


Figure 8. Diode Rectifier

AC/DC/AC configuration has following features:

- The motor can operate at a higher speed without field weakening (by maintaining the DC-bus voltage above the supply voltage peak),
- Common mode voltage decreases by one-third compared to conventional configuration due to the simultaneous control of rectifier – inverter (same switching frequency and synchronized sampling time may avoid common mode voltage pulse because the different type of zero voltage (*U0,U7*) are not applied at the same time) .

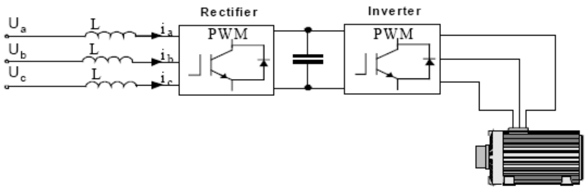


Figure 9. AC/DC/AC converter

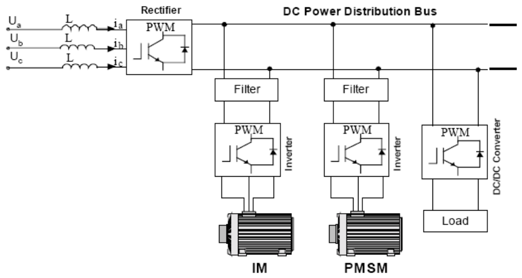


Figure 10. DC distributed Power System

IV. PACE VECTOR MODULATION

The SVM strategy based on space vector representation (Fig. 9) becomes very popular due to its simplicity. A three-phase two-level converter provides eight possible switching states, made up of six active and two zero switching states. Active vectors divide plane for six sectors, where a reference vector *U** is obtained by switching on (for proper time) two adjacent vectors. It can be seen that vector *U** (Fig. 10) is possible to implement by the different switch on/off sequence of *U1* and *U2*, and that zero vectors decrease modulation index. Allowable length of *U** vector, for each of α angle, is equal *U*max =*Udc*/ 3

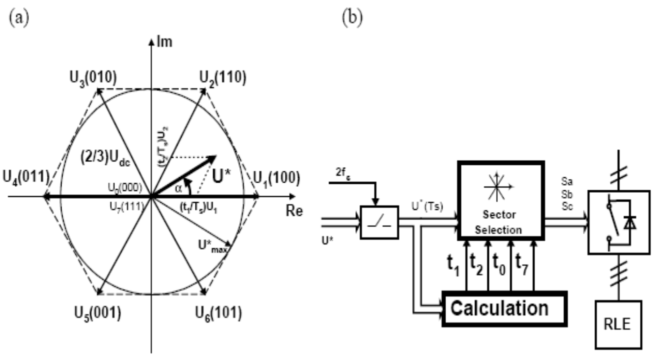


Figure 11. (a) Space vector representation of three-phase converter, (b) Block diagram of SVM

Contrary to *CB-PWM*, in the *SVM* there is no separate modulator for each phase. Reference vector *U** is sampled with fixed clock frequency *2fs = 1/Ts*, and next *U*(Ts)* is used to solve equations which describe times *t1*, *t2*, *t0* and *t7* (Fig. 11). Microprocessor implementation is described with the help of simple trigonometrical relationship for first sector , and, recalculated for the next sectors (n).

$$t_1 = \frac{2\sqrt{3}}{\pi} MT_S \sin(\pi/3-\alpha) \quad (3.1a)$$

$$t_2 = \frac{2\sqrt{3}}{\pi} MT_S \sin(\alpha) \quad (3.1b)$$

After *t1* and *t2* calculation, the residual sampling time is reserved for zero vectors *U0*, *U7* with condition *t1 + t2 ≤ Ts*. The equations (3.1a), (3.1b) are identical for all variants of *SVM*. The only difference is in different placement of zero vectors *U0 (000)* and *U7 (111)*. It gives different equations defining *t0* and *t7* for each of method, but total duration time of zero vectors must fulfill conditions:

$$t_{0,7} = T_S - t_1 - t_2 = t_0 + t_7 \quad (3.2)$$

The neutral voltage between *N* and *0* points is equal: (see Tab. 3.2)

$$U_{N0} = \left(-\frac{U_{dc}}{2}t_0 - \frac{U_{dc}}{6}t_1 + \frac{U_{dc}}{6}t_2 + \frac{U_{dc}}{2}t_7\right) = \frac{U_{dc}}{2}\left(-t_0 - \frac{t_1}{3} + \frac{t_2}{3} + t_7\right) \quad (3.3)$$

TABLE I. THREE-PHASE SVM WITH SYMMETRICAL PLACEMENT OF ZERO VECTORS (SVPWM)

	U_{a0}	U_{b0}	U_{c0}	U_{aN}	U_{bN}	U_{cN}	U_{NO}
U_0	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	0	0	0	$-U_{dc}/2$
U_1	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	$2U_{dc}/3$	$-U_{dc}/3$	$-U_{dc}/3$	$-U_{dc}/6$
U_2	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/3$	$U_{dc}/3$	$-2U_{dc}/3$	$U_{dc}/6$
U_3	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/3$	$2U_{dc}/3$	$-U_{dc}/3$	$-U_{dc}/6$
U_4	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-2U_{dc}/3$	$U_{dc}/3$	$U_{dc}/3$	$U_{dc}/6$
U_5	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/3$	$-U_{dc}/3$	$2U_{dc}/3$	$-U_{dc}/6$
U_6	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/3$	$-2U_{dc}/3$	$U_{dc}/3$	$U_{dc}/6$
U_7	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	0	0	0	$U_{dc}/2$

V. HYSTERESIS CURRENT CONTROLLER

Among the conventional current-controlled schemes, the hysteresis current control provides a simple and robust current control performance with good stability; very fast response and an inherent ability to control peak current.

A. Conventional Hysteresis Current Control

For three-phase, three-level PWM rectifier systems the CHC, is implemented independently for each phase. Each current controller directly generates the switching signal, *si'*, where *i*indicates the phase *R*, *S* or *T*. For the case of positive input current, if the error between the phase currentand the reference sinusoidal current, exceeds the upper hysteresis limit *+h*, the power transistor of the corresponding phase is turned off, causing $i_i$to decrease. Once $i_i$reaches the lower hysteresis limit *–h*, the power transistor is turn on again, the phase current increases and the cycle repeats.

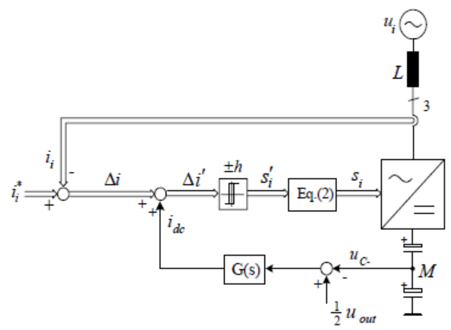


Figure 12. Block diagram and simulated rectifier input phase current for conventional hysteresis current control (CHC).

$$s_i' = \begin{cases} 0 & if \quad i_i > i_i^* + h \\ 1 & if \quad i_i < i_i^* - h \end{cases}$$

The final switching decision, *si*, is determined considering the direction of the mains phase current [8] or the sign of the corresponding reference current i_i* as given in (2) or of the related mains phase voltage $ui(i_i*\sim u_i)$.

$$s_i = \begin{cases} s_i' & if \quad i_i^* \geq 0 \\ NOT\ s_i' & if \quad i_i^* < 0 \end{cases} .$$

B. Conventional Carrier-based Current Control

For CCC, the switching decision *si'*, is the result of a comparison of the dynamically weighted current error (in the simplest case only a Ptype control is employed) with a triangular carrier signal. The use of a triangular carrier results in a constant switching frequency.

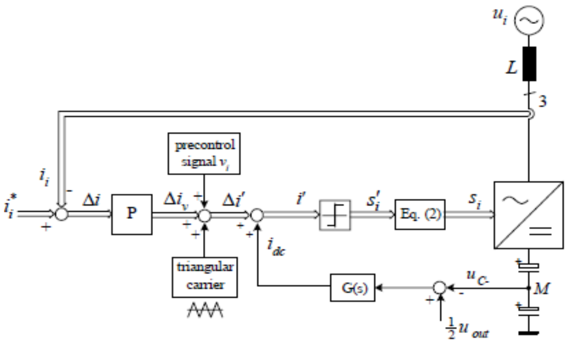


Figure 13. Block diagram for conventional carrier-based current control (CCC).

As with the hysteresis control, the final switching decision, *si*, depends on the sign of the corresponding mains phase current reference value. In order to ensure a low current control error and/or a sinusoidal input current shape also for P-type control, a mains voltage precontrol signal, *vi*, is added to the current controller output. The time behavior of the pre-control signal can be derived from an analysis of the input voltage formation resulting in

$$v_i' = \begin{cases} \hat{I}_{CS}\left(\dfrac{4u_i}{U_{out}} - 1\right) & if\ i_i \geq 0 \\ \hat{I}_{CS}\left(\dfrac{4u_i}{U_{out}} + 1\right) & if\ i_i < 0 \end{cases}$$

(*ÎCS* represents the amplitude of the triangular carrier signal) which then is extended by a third harmonic, *vi = vi´+ u3* (*u3*= 2 1 (*max* {*uR, uS, uT*} + *min* {*uR, uS, uT*})) in order to allow a full utilization of the modulation range. As the output voltage center point of the rectifier for CCC is naturally stable, theoretically no output voltage center point control would have to be provided. However, in a practical realization an asymmetry of the partial output voltages can occur due to non idealities such as different switching and gate drive delay times of the phases. Therefore, a control of the center point voltage is implemented following the same concept as for the CHC. For the switching state sequence of the CCC a subsequent rectifier switching state is achieved by changing always only the switching state of one phase. Compared to that the switching of the CHC is highly irregular, what results in a higher average switching frequency for equal input current ripple rms value.

Hysteresis Current Controller (HCC) has been a very popular current control technique, owing to its easy implementation, fast dynamic response, maximum current limit, and insensitivity to load parameter variation. However, it suffers from the drawbacks of random switching and excessively large switching hand.

VI. SPACE VECTOR MODULATION BASED HYSTERESIS CURRENT CONTROLLER

Space vector modulation (SVM) technique was first introduced by German researchers in the mid of 1980s. This technique showed several advantages over the traditional PWM technique and has been proven to inherently generate superior PWM waveforms. By implementing the SVM technique, the number of switching is reduced to about 30% at the same carrier frequency of the sinusoidal pulse width modulation (SPWM) method. It offers better DC bus utilizations with lower THD in the AC current and reduces of switching losses too.

The SVM based hysteresis current controller inherits all the advantages of the hysteresis control and SVM technique. This configuration can reduce the switching losses by implementing SVM techniques and produce a better current shape by using a significant tolerance bandwidth of the hysteresis control. This switching technique has been implemented in a three phase inverter drives applications and also in a three phase rectifiers. As a result, this SVM technique can overcome the coordination problems of the hysteresis current control by calculating the switching vectors of the voltage source converter or the active filter. Besides that, the hardware implementation of the SVM based current controllers are easier compared to the conventional PWM technique, as the space vectors equations are represented by logic operation.

VII. SIMULATION DESCRIPTION

The simulation was carried out using MATLAB Simulink software. The Simulink designed is easy to understand. The three phase supply voltage is given to the PWM rectifier through the inductance. The three voltages are measured and are given to the mux and then to the PLL. The three multipliers are implemented to multiply the cosine function, output of SVM and the PID output. The PID controller is used to control the error voltage. The hysteresis controller is implemented to control the current limit by comparing the current reference and the input current. The output is given to the demux and the output of this demux gives the gate pulses. The gate pulses to the IGBT switches. The output is taken across the R load.

The simulation parameters are,

TABLE II. INPUT PARAMETERS AND VALUES

Parameters	Given Values
Input phase voltage	110 volts
Source boost inductance	5 mH
DC bus capacitor	3200 µF
Output resistor	50 Ω
Inductance	50 mH
Capacitance	2200 µF
Reference load voltage	400 volts

The space vector modulation simulink model consists of xyz calculator subsystem model and sector selector subsystem. The three phase input supply is converted into the xyz axis. In the sector selector switch the first port is the control pin. According to the control data, the region is selected. Here, special care is taken in the division of regions. The output is given to three multipliers.

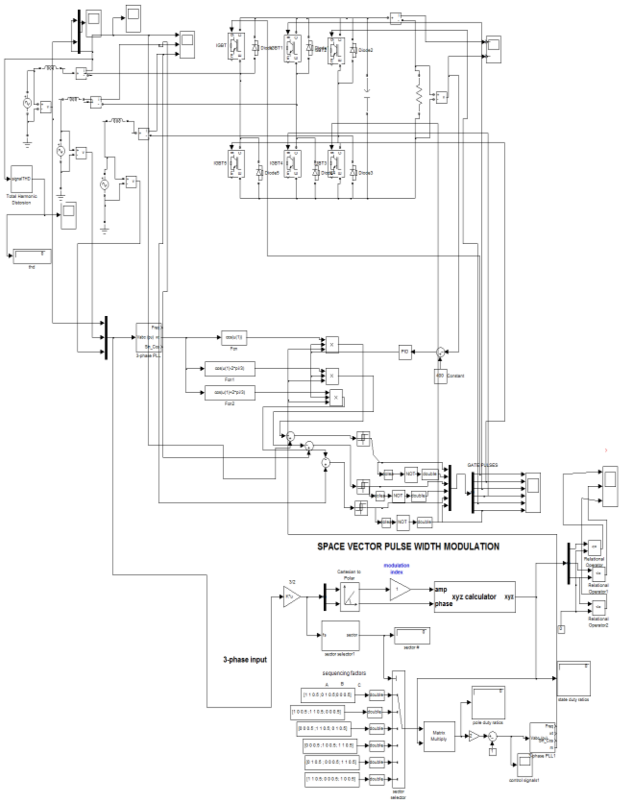


Figure 14. Simulink model for SVM-Based HCC Controller

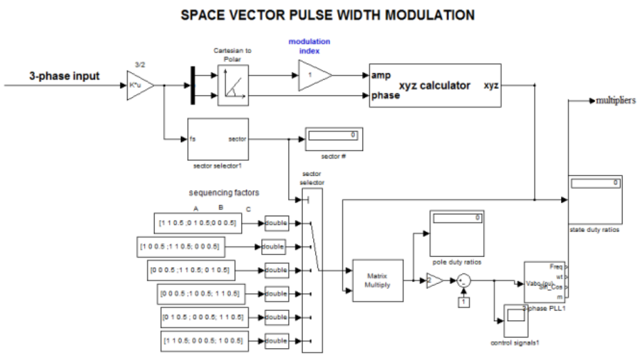


Figure 15. Space vector modulation simulink model

The simulink model to find the xyz calculator is shown in the above model. This is a subsystem model used in the space vector modulation. Initially 'mod' function is used to obtain the alpha value. Two multipliers are used here to multiply the amplitude and the angle. Thus x, y and z axis are obtained by using this simulink model. The switch selects the first port if it satisfies the control criterion, otherwise the third port is selected.

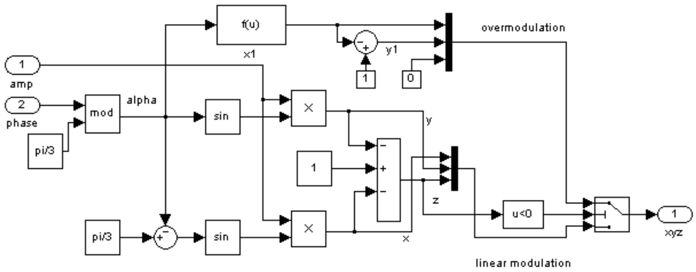


Figure 16. Simulink model to find xyz calculator

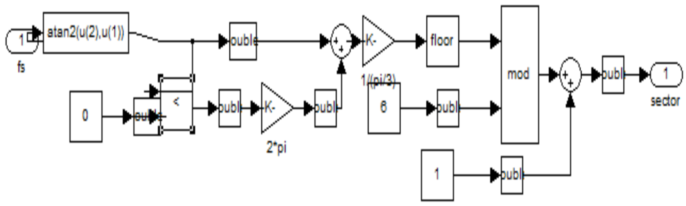
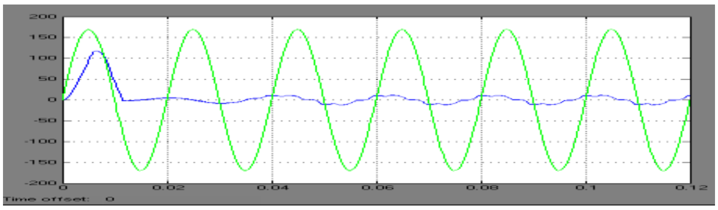


Figure 17. Simulink model to find sector selector

The above simulink model is used to find the sector. This is also a subsystem used in the space vector modulation. The link used is simpler to design, implement and to obtain the result.

VIII. SIMULATION RESULTS



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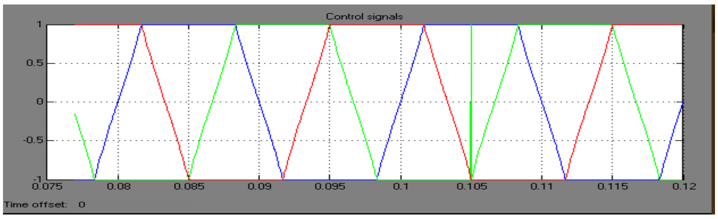

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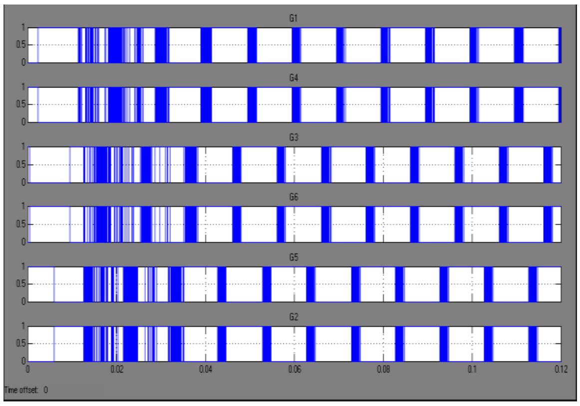

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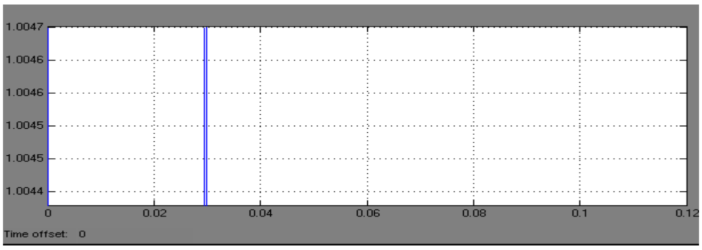
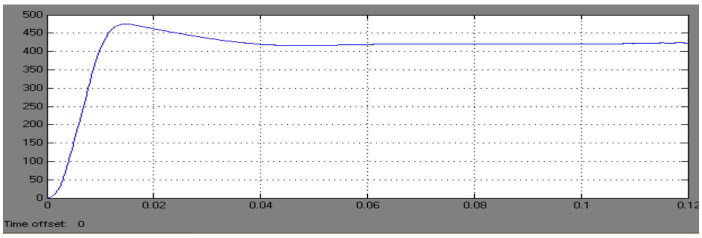
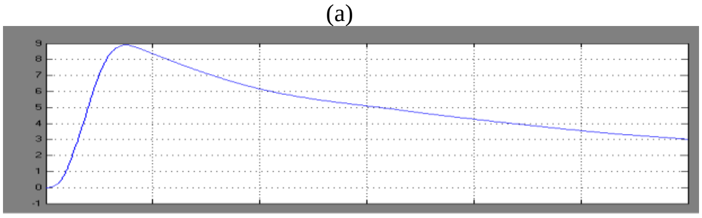


Figure 18. (a) Phase 'a' Source Voltage and Current waveforms (b) Simulink result of the control signals (c) Gate signals (d)THD of phase current

A. For R-L-C load:



(a)



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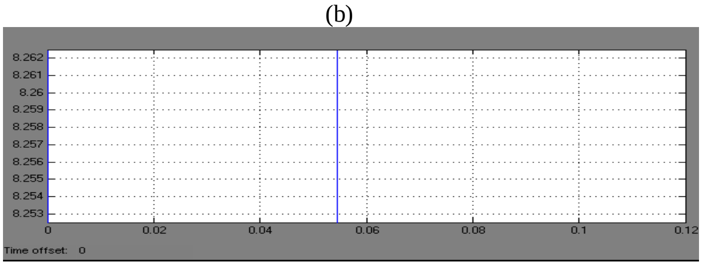

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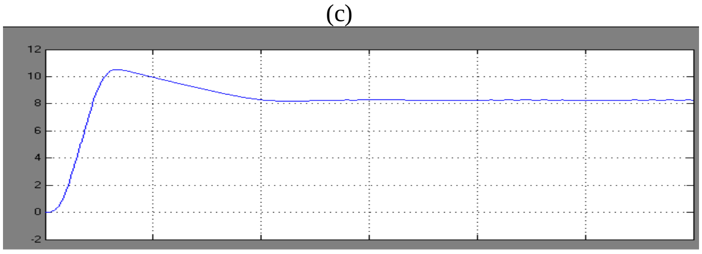

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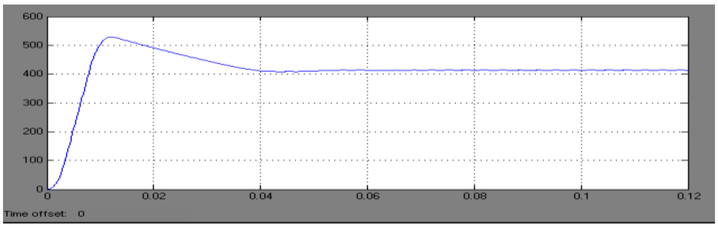

(e)

Figure 19. (a)Output Voltage of SVM&HCC based Rectifier Model for R-L-C load (b) Load current for R-L-C load (c) THD of load current for R-L load (d) Output waveform of load current for both R-L and R load (e) Output Voltage of SVM&HCC based Rectifier Model for R and R-L load

IX. CONCLUSION

Thus, the technique adopted utilizes all the advantages of SVM & HCC. The converter operates at a relatively lower switching frequency than the conventional HCC-based converter and thus gives reduced switching power losses and higher conversion efficiency. The current controller confines the state space vectors from the region detector and applies a proper space vector selected according to HCC, for a better current wave shape. Since the output is ripple free, it is undoubtedly used in telecommunications and power supplies.

X. FUTURE PROPOSAL

This paper is considered for low switching frequency. As an extension, this paper is proposed to analyze at various frequencies in the future. Selective harmonics can be eliminated by using microcontroller.

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